

Listing of the Claims

1. (Currently Amended) A security module for protecting circuit components from unauthorized access, the module comprising:

a substrate composed of a plurality of layers including a first layer, the first layer of the substrate for supporting circuit components to be protected;

a cover member composed of a plurality of layers, the cover member having a surface for abutting the first layer of the substrate, the cover member defining an enclosure space for enclosing circuit components to be protected between the cover member and the substrate, when the circuit components are supported on the substrate and the cover member is abutted to the substrate; and

a sensor comprising at least one conduction path disposed in and integral to at least one of the layers below the first layer of the substrate and at least one conduction path disposed in and integral to at least one of the layers of the cover member.

2. (Original) The security module as recited in claim 1, further comprising an electronic circuit disposed on the substrate for detecting at least one of a short or a break in the conduction path disposed in the substrate or in the cover member.

3. (Original) The security module as recited in claim 1, wherein the conduction path in the substrate and the cover member comprise at least one serpentine path.

4. (Original) The security module as recited in claim 1, wherein the conduction path in the substrate and the cover member comprises a plurality of serpentine paths.

5. (Original) The security module as recited in claim 1, wherein the substrate and the cover member comprise a plurality of layers, each layer having at least one conduction path.

6. (Original) The security module as recited in claim 5, wherein each layer of the substrate and the cover member comprises a plurality of serpentine paths.

7. (Original) The security module as recited in claim 6, wherein the plurality of serpentine paths are disposed on the substrate and the cover member in a pseudo-random configuration.

8. (Original) The security module as recited in claim 1, each conduction path comprising a thin-film conductor formed directly on the associated layer.

9. (Original) A security module as recited in claim 1, wherein:

the cover member has side portions and a lid portion, the lid portion disposed over and spaced from the top layer of the substrate, when the cover member is abutted to the substrate;

the at least one conduction path in the layers of the cover member comprise at least one conduction path in the sensor;

the sensor further comprising a plurality of vias disposed in the side portions of the cover member, each via comprising an electrically conductive material connecting at least one conduction path in the layers of the cover member to the surface of the cover member.

10. (Original) A security module as recited in claim 9, the sensor further comprising:

a plurality of vias disposed along a periphery of the substrate, each via comprising an electrically conductive material connecting at least one conduction path in the layers of the substrate to the first layer of the substrate.

11. (Original) The security module recited in claim 10, wherein the plurality of vias are disposed along the periphery of the substrate in a staggered pattern.

12. (Original) A security module for protecting circuit components from unauthorized access, the module comprising:

a substrate for supporting circuit components to be protected, the substrate having a first surface;

a cover member including side portions defining a second surface for abutting the first surface of the substrate, the cover member defining an enclosure space for enclosing circuit components to be protected between the cover member and the substrate and surrounded by the side portions of the cover member, when the circuit components are supported by the substrate and the second surface of the cover member is abutted to the first surface of the substrate; and

a sensor comprising a plurality of vias in the side portions of the cover member, each via comprising an electrically conductive material defining a plurality of conduction paths extending transverse to the first and second surfaces, surrounding the enclosure space, when the second surface of the cover member is abutted to the first surface of the substrate.

13. (Original) The security module recited in claim 12, wherein the plurality of vias in the side portions of the cover member are disposed in a staggered pattern.

14. (Original) A security module for protecting circuit components from unauthorized access, the module comprising:

a substrate for supporting circuit components to be protected, the substrate having a first surface;

a cover member including side portions defining a second surface for abutting the first surface of the substrate, the cover member defining an enclosure space for enclosing circuit

components to be protected between the cover member and the substrate and surrounded by the side portions of the cover member, when the circuit components are supported by the substrate and the second surface of the cover member is abutted to the first surface of the substrate; and

a sensor comprising a plurality of solder balls electrically connected to the second surface of the cover member, the plurality of solder balls electrically and mechanically connecting to the first surface of the substrate when the second surface of the cover member is abutted to the first surface of the substrate.

15. (Original) The security module in claim 14, the sensor further comprising:

a plurality of surface interconnects disposed on the abutting surfaces of both the substrate and the cover member, at least one of the plurality of surface interconnects on both the substrate and the cover member being electrically connected to at least one of the plurality of solder balls, the plurality of surface interconnects on the substrate and the cover member having matching patterns that electrically interconnect when the second surface of the cover member is abutted to the first surface of the substrate;

16. (Original) The security module recited in claim 15, the sensor further comprising

a plurality of surface serial conductors on the abutting surfaces of both the substrate and the cover member, at least one of the plurality of surface serial conductors on both the substrate

and the cover member electrically interconnecting the plurality of surface interconnects on the respective abutting surfaces of the substrate and cover member.

17. (Original) The security module recited in claim 15, wherein:

the substrate and the cover member each comprise one or more and, preferably, a plurality of layers, at least one of the plurality of layers on both the substrate and the cover member having at least one conduction path disposed thereon, the at least one conduction path being electrically connected to at least one of the plurality of solder balls.

18. (Withdrawn) A method for manufacturing a security module, the method comprising the steps of:

providing a substrate, the substrate composed of a plurality of layers including a first layer, the first layer of the substrate for supporting circuit components to be protected;

providing a cover member, the cover member composed of a plurality of layers, the cover member having a surface for abutting the first layer of the substrate, the cover member defining an enclosure space for enclosing circuit components to be protected between the cover member and the substrate, when the circuit components are supported on the substrate and the cover member is abutted to the substrate;

providing a sensor comprising at least one conduction path disposed in at least one of the layers below the first layer of the substrate and at least one conduction path disposed in at least one of the layers of the cover member.

19. (Withdrawn) The method recited in claim 18, wherein the step of providing a sensor comprising at least one conduction path disposed in at least one of the layers below the first layer of the substrate and at least one conduction path disposed in at least one of the layers of the cover member comprises forming a thin-film conductor directly on the associated layer.

20. (Withdrawn) The method recited in claim 19, wherein the step of forming a thin-film conductor directly on the associated layer further comprises forming a plurality of thin-film conductors on the associated layer.

21. (Withdrawn) The method recited in claim 20, wherein the plurality of thin-film conductors are formed on the associated layer in a pseudo-random configuration.

22. (Withdrawn) The method recited in claim 18, further comprising the step of:

providing a plurality of vias in the side portions of the cover member, each via comprising an electrically conductive material connecting at least one conduction path in the layers of the cover member to the surface of the cover member.

23. (Withdrawn) The method recited in claim 22, wherein the plurality of vias in the side portions of the cover member are formed in a staggered configuration.

24. (Withdrawn) The method recited in claim 22, further comprising the step of:

providing a plurality of vias along a periphery of the substrate, each via comprising an electrically conductive material connecting at least one conduction path in the layers of the substrate to the first layer of the substrate.

25. (Withdrawn) The method recited in claim 24, wherein the plurality of vias along the periphery of the substrate are formed in a staggered configuration.

26. (Withdrawn) The method recited in claim 24, further comprising the step of:

providing a plurality of surface interconnects disposed on the abutting surfaces of both the substrate and the cover member, the plurality of surface interconnects on the substrate and the cover member having matching patterns that electrically interconnect when the cover member is

abutted to the substrate, and wherein at least one of the plurality of surface interconnects is electrically connected to at least one of the plurality of vias in the cover member and the substrate.

27. (Withdrawn) The method recited in claim 26, further comprising the step of:

providing a plurality of surface serial conductors on the abutting surfaces of both the substrate and the cover member, at least one of the plurality of surface serial conductors on both the substrate and the cover member electrically interconnecting the plurality of surface interconnects on the respective abutting surfaces of the substrate and cover member.

28. (Withdrawn) The method recited in claim 27, wherein the step of providing a plurality of surface serial conductors on the abutting surfaces of both the substrate and the cover member comprises utilizing a thin solder mask to form the surface serial conductors.

29. (Withdrawn) The method recited in claim 27, further comprising the step of:

providing a plurality of solder balls, at least one of the plurality of solder balls being electrically connected to at least one of the plurality of surface interconnects on the cover member.

30. (Withdrawn) The method recited in claim 29, wherein the step of providing a plurality of solder balls comprises printing a eutectic alloy over a pattern of the surface interconnects on the cover member and reflowing to form the solder balls.

31. (Withdrawn) The method recited in claim 29, further comprising the step of:
abutting the surfaces of the substrate and the cover member together.

32. (Withdrawn) The method recited in claim 31, wherein the abutting step comprises aligning the
plurality of solder balls on the cover member with the plurality of surface interconnects on the substrate and reflowing the assembly.

33. (Withdrawn) The method recited in claim 29, further comprising the step of:
providing a pseudo-randomly configured three-dimensional resistive network by electrically interconnecting at least one conduction path, at least one via, at least one surface interconnect, at least one surface serial conductor, and at least one solder ball.

34. (Withdrawn) The method recited in claim 33, wherein the step of electrically interconnecting at least one conduction path, at least one via, at least one surface interconnect, at

Applicants: Justin H. BENSON *et al.*
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least one surface serial conductor, and at least one solder ball comprises wirebonding a programmable pad array.